IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Previously Presented): A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and a third semiconductor layer of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$$0 < A = t / (t+d) \leqq 0.72$$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein, assuming that a breakdown voltage is represented by VB (V), then t, VB (V), and A satisfy a relationship below:

$$t < 2.53 \times 10^{-6} \times (A \times VB)^{7/6} \text{ (cm)}.$$

Claim 2 (Original): A semiconductor device according to claim 1, wherein, assuming that an aspect ratio B is represented by B = d/w, where w is an interval between adjacent third semiconductor layers, the layer thickness ratio A and the aspect ratio B satisfy an expression below:

$$A \times B \leqq 1.15.$$

Claim 3 (Original): A semiconductor device according to claim 1, wherein an aspect ratio B and the layer thickness ratio A satisfy an expression below:

$$-0.04B + 0.48 < (A \times B) < 0.13B + 0.59$$

where the aspect ratio B is represented by B = d/w, and w is an interval between adjacent third semiconductor layers.

Claim 4 (Original): A semiconductor device according to claim 1, wherein a product of A × B satisfies a relationship below:

$$0.58 < (A \times B) < 0.71$$

wherein B denotes the an aspect ratio represented by B = d/w, where w is an interval between adjacent third semiconductor layers.

Claim 5 (Canceled).

Claim 6 (Original): A semiconductor device according to claim 3, wherein, assuming that an impurity concentration of the first semiconductor layer is represented by Nn and that a breakdown voltage is represented by VB (V), then Nn, VB (V), and A satisfy the relationship below:

$$Nn > 1.11 \times 10^{18} \times (A \times VB)^{-4/3} \text{ (cm-3)}.$$

Claim 7 (Original): A semiconductor device according to claim 1, wherein an insulating material is interposed between the second semiconductor layer and the third semiconductor layer.

Claim 8 (Original): A semiconductor device according to claim 7, wherein a void is present in said insulating material.

Claim 9 (Original): A semiconductor device according to claim 1, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 10 (Original): A semiconductor device according to claim 2, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 11 (Original): A semiconductor device according to claim 3, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 12 (Original): A semiconductor device according to claim 4, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 13 (Original): A semiconductor device according to claim 5, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 14 (Original): A semiconductor device according to claim 6, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 15 (Original): A semiconductor device according to claim 7, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 16 (Original): A semiconductor device according to claim 8, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 17 (Original): A semiconductor device according to claim 1, wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer.

Claim 18 (Original): A semiconductor device according to claim 17, wherein a plurality of voids are present independently along the border region.

Claim 19 (Original): A semiconductor device according to claim 17, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 20 (Original): A semiconductor device according to claim 18, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 21 (Currently Amended): A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and [[a]] at least two third semiconductor layers ~~layer~~ of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$$0 < A = t / (t+d) \leqq 0.72$$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein insulating films are interposed ~~every border regions~~ between the second semiconductor layer and third semiconductor layers.

Claim 22 (Previously Presented): A power semiconductor device, comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of the first conductivity type and a third semiconductor layer of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode electrically in contact with the first semiconductor layer;

a fourth semiconductor layer of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer; and a layer thickness ratio A is given by an expression:

$$0 < A = t / (t+d) \leqq 0.72$$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer.

Claim 23 (Previously Presented): The semiconductor device according to claim 21, wherein a void is present in said insulating films.

Claim 24 (Currently Amended): A semiconductor device according to claim 21, wherein an impurity concentration profile of at least one of the second semiconductor layer and the at least two third semiconductor layers ~~layer~~ gradually reduces with depth.

Claim 25 (Currently Amended): A semiconductor device according to claim 23, wherein an impurity concentration profile of at least one of the second semiconductor layer and the at least two third semiconductor layers ~~layer~~ gradually reduces with depth.

Claim 26 (Previously Presented): A semiconductor device according to claim 22, wherein a plurality of voids are present independently along the border region.

Claim 27 (Previously Presented): A semiconductor device according to claim 22, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.

Claim 28 (Currently Amended): A semiconductor device according to claim [[27]] 23, wherein an impurity concentration profile of at least one of the second semiconductor layer and the third semiconductor layer gradually reduces with depth.